

A few highlights on small systems ...

Brian DeLacey

April 15, 2015

BLU at MIT

Night Vision and Electronic Sensors

*Imaging systems are increasingly embedding processing power
... as just one example of how SOCs and computational power is everywhere*



CERDEC's Night Vision and Electronic Sensors Directorate researches and develops sensor and sensor suite technologies for air and ground intelligence, surveillance, reconnaissance and target acquisition under adverse battlefield conditions in day and night-time environments.


NIGHT VISION AND ELECTRONIC SENSORS DIRECTORATE

CERDEC's Night Vision and Electronic Sensors Directorate, located at **Fort Belvoir, Va.**, is "The Army's Sensor Developer," conducting research and development that provides U.S. Soldiers with advanced sensor technology to dominate the 21st-century digital battlefield.

http://www.cerdec.army.mil/inside_cerdec/nvesd/

Embedded Vision

ECE Colloquium Series



Nibir K. Dhar
Chief Scientist
Night Vision Electronic Sensors Directorate

- ▶ April 15, 2015 (Wed.) 4pm
- ▶ 8 St. Mary's St., PHO 211
- ▶ Faculty Host: Enrico Bellotti

Light refreshments will be near PHO 211 at 3:45 pm.

Imaging Technology: What is on the Horizon?

Advances in imaging technology have huge impact on our daily lives. Innovations in optics, focal plane arrays (FPA), microelectronics, photonics and computation have revolutionized camera design. As a result, new approaches to camera design and low cost manufacturing is now possible. These advances are clearly evident in visible wavelength band due to pixel scaling, improvements in silicon material and CMOS technology. CMOS cameras are available as "embedded vision" products in cell phones and many other consumer products. Advances in infrared imaging technology have been slow due to market volume and many technological barriers in detector materials, optics and fundamental limits imposed by the pixel scaling and optics. There is of course much room for innovation in both, visible and infrared imaging technology. This presentation will highlight a few of the imaging technology challenges and related projects at NVESD and DARPA/MTO office. In particular, description of new technology development in scalable camera architecture, IR pixel scaling, broadband and multiband FPAs for day/night applications and low cost manufacturing of thermal imaging technology will be discussed. A new trend in "embedded vision" will also be discussed.

To Learn More:
bu.edu/ece/calendar

BOSTON UNIVERSITY Boston University College of Engineering
Department of Electrical & Computer Engineering



Imaging chips and algorithms for smartphones and other camera devices

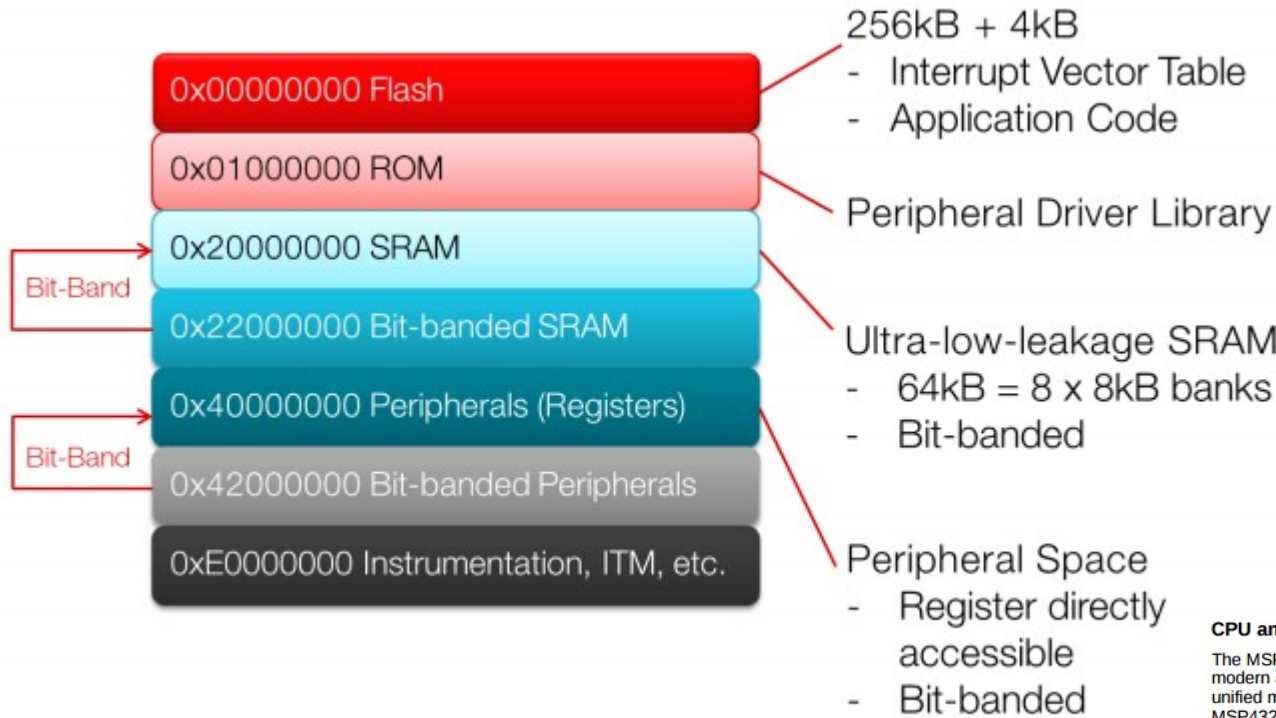
<http://www.dxo.com/us/embedded-imaging/image-signal-processor-isp>

Nibir K. Dhar, Chief Scientist, Night Vision Electronic Sensors Directorate, Faculty Host: Enrico Bellotti. Light Refreshments will be available outside of room 211 at 3:45 pm. -- Imaging Technology: What is on the Horizon? -- Abstract: Advances in imaging technology have huge impact on our daily lives. Innovations in optics, focal plane arrays (FPA), microelectronics, photonics and computation have revolutionized camera design. As a result, new approaches to camera design and low cost manufacturing is now possible. These advances are clearly evident in visible wavelength band due to pixel scaling, improvements in silicon material and CMOS technology. CMOS cameras are available as "embedded vision" products in cell phones and many other consumer products. Advances in infrared imaging technology have been slow due to market volume and many technological barriers in detector materials, optics and fundamental limits imposed by the pixel scaling and optics. There is of course much room for innovation in both, visible and infrared imaging technology.

<http://www.bu.edu/calendar/?uid=167728@17.calendar.bu.edu>

<http://www.nvl.army.mil/>

MSP432



<http://www.ti.com/tool/MSP-EXP432P401R>

Figure 4. MSP432 Memory Map (MSP432P401R)

CPU and Core

The MSP430 CPU is a 16-bit RISC architecture that incorporates features specifically designed for modern and efficient programming such as orthogonal architecture, single-cycle register instruction, unified memory map with no paging, and direct memory-to-memory transfer, just to name a few. The MSP432 CPU is built around the industry standard ARM Cortex-M4F 32-bit core and benefits from the complete ecosystem of development tools and software solutions associated with ARM processors. Although they may be perceived as radically different, these two processors indeed share many architectural similarities summarized in Table 1.

Table 1. MSP430 and MSP432 Core Comparison

| Name | MSP430 | MSP432 |
|-----------------------------|---|--|
| Data size | 16 bit | 32 bit |
| Program bus width | 16-bit (CPU) or 20-bit (CPUX) address bus | 32 bit |
| Bus type | 16-bit MSP430 bus | AHB |
| Architecture | Von Neumann (Princeton): data op and instruction fetch share same bus | Harvard: separate data and instruction buses |
| Instruction Set | RISC, MSP430 proprietary | RISC, thumb and thumb2 |
| Instruction size | 16-bit (and 16-bit for each operand) | 16-bit and 32-bit |
| Instruction Cycle (typical) | 1-4 cycles | 1-2 cycles |
| Pipeline | None | 3-stage pipeline |
| Prefetch buffer | 128 bit | 128 bit |
| Power Modes | Active, LPM0-LPM4, LPMx.5 | Active, Low Frequency, LPM0, LPM3, LPMx.5 |
| Debug Interface | MSP430 4-wire JTAG, and 2-wire SBW | ARM JTAG in 4-wire and 2-wire modes |
| Math support | Hardware Multiplier (MPY) | Hardware Multiplier and Divider, DSP extension, and integrated FPU |

<http://www.ti.com/lit/an/slaa656/slaa656.pdf>

MSP432 Functional Diagram

<http://www.ti.com/lit/ds/slas826a/slas826a.pdf>



1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the MSP432P401x devices.

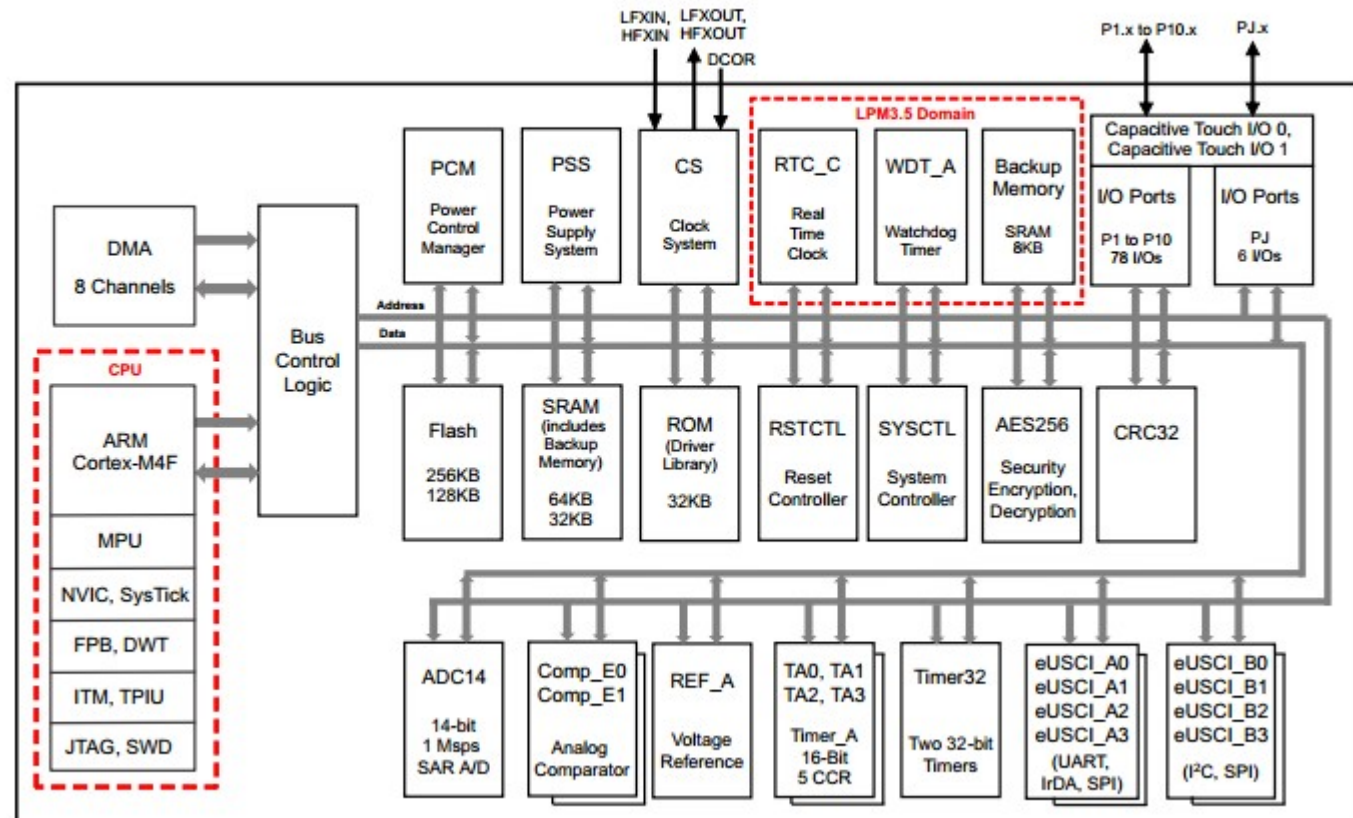


Figure 1-1. MSP432P401x Functional Block Diagram

<http://letsmakerobots.com/content/msp432p401x-vs-tm4c123gh6pm-texas-instruments-microcontrollers-a-brief-review>

TI-RTOS

WHITE PAPER

Nick Lethaby
OS Product Manager
Texas Instruments Incorporated

Introduction



TEXAS INSTRUMENTS

Why Use a Real-Time Operating System in MCU Applications

Energia MultiTasking



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Multitasking

Multitasking is the ability to run multiple tasks or threads concurrently on a microcontroller. In Energia MT, multitasking is achieved by treating each tab as a separate task and letting TI-RTOS and Energia take care of the rest. Currently, Multitasking is supported on the MSP432 launchpad.

Setting up Multitasking applications in Energia MT

Each tab in Energia MT will be treated as a new task, assuming the tab has a `setup()` and `loop()` function with a matching and unique name. For example, an application with 2 tasks could be called `setupTask1()/loopTask1()` and `setupTask2()/loopTask2()`. Energia MT will look for these keyword pairs and automatically turn them into tasks.

TI SensorTag

Features of the new TI SensorTag

- » More sensors
 - Added support for more low-power sensors
 - 10 sensors including support for light, microphone, and magnetic sensors
- » Lower power
 - Peak power consumption reduced by 75%
- » Significantly improved performance with ARM Cortex-M3 (CC2650 wireless MCU)
- » Multi-standard wireless support
 - Bluetooth Smart
 - ZigBee®
- » Cloud connectivity
 - Access and control your SensorTag from anywhere
 - Seamless integration with mobile apps and web through cloud services
- » Complete development system
 - Low-cost debugger/emulator add-on available
 - Code Composer™ Studio compiler license included

SensorTag App

- » Available for both Android and iOS
- » [Source code available for download](#)
- » Build your own SensorTag app in minutes by enabling the SensorTag sensors
- » Quick and easy prototyping

<http://www.ti.com/tool/cc2650stk>



Questions?

Follow-on session in more detail next month

May 20, 2015

BLU @ MIT

“Energia MT: Efficiently Sensing the World Around You”

<http://blu.org/cgi-bin/calendar/2015-may>