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BLU - 2020/05/20

Outline

- Ryzen product family
- Zen CPUs
- Ryzen architecture
  - Chiplets
- Ryzen APUs

Ryzen Products

- Ryzen Desktop products
  - CPUs and APUs
  - Threadripper
- Ryzen Mobile
  - For laptops – usually are all APUs
- Ryzen Embedded

CPU Product Nomenclature

- Zen core - 14nm
  - Ryzen 3/5/7 1xxx (Summit Ridge)
  - Threadripper 19xx
- Zen+ core - 12nm
  - Ryzen 3/5/7 2xxx (Pinnacle Ridge)
  - Threadripper 29xxx
- Zen2 core – 7nm CCD
  - Ryzen 3/5/7/9 3xxx (Matisse)
  - Threadripper 39xx

APU Product Nomenclature

- Zen core, Vega GFX (“Raven Ridge”)
  - Desktop: Ryzen (Pro) 3/5 2xxxG
  - Mobile: Ryzen (Pro) 3/5/7 2xxxU/H
- Zen+ core, Vega GFX (“Picasso”)
  - Desktop: Ryzen (Pro) 3/5 3xxxG
  - Mobile: Ryzen (Pro) 3/5/7 3xxxU/H
- Zen2 core, Vega GFX (“Renoir”)
  - Desktop: Not yet released
  - Mobile: Ryzen (Pro) 3/5/7 4xxxU/H

Cool Fact

- All Zen/Zen+/Zen2 based desktop products are socket AM4 compatible
  - Applies to both CPUs and APUs
  - Also to monolithic APU dies as well as new chiplet architecture in Matisse
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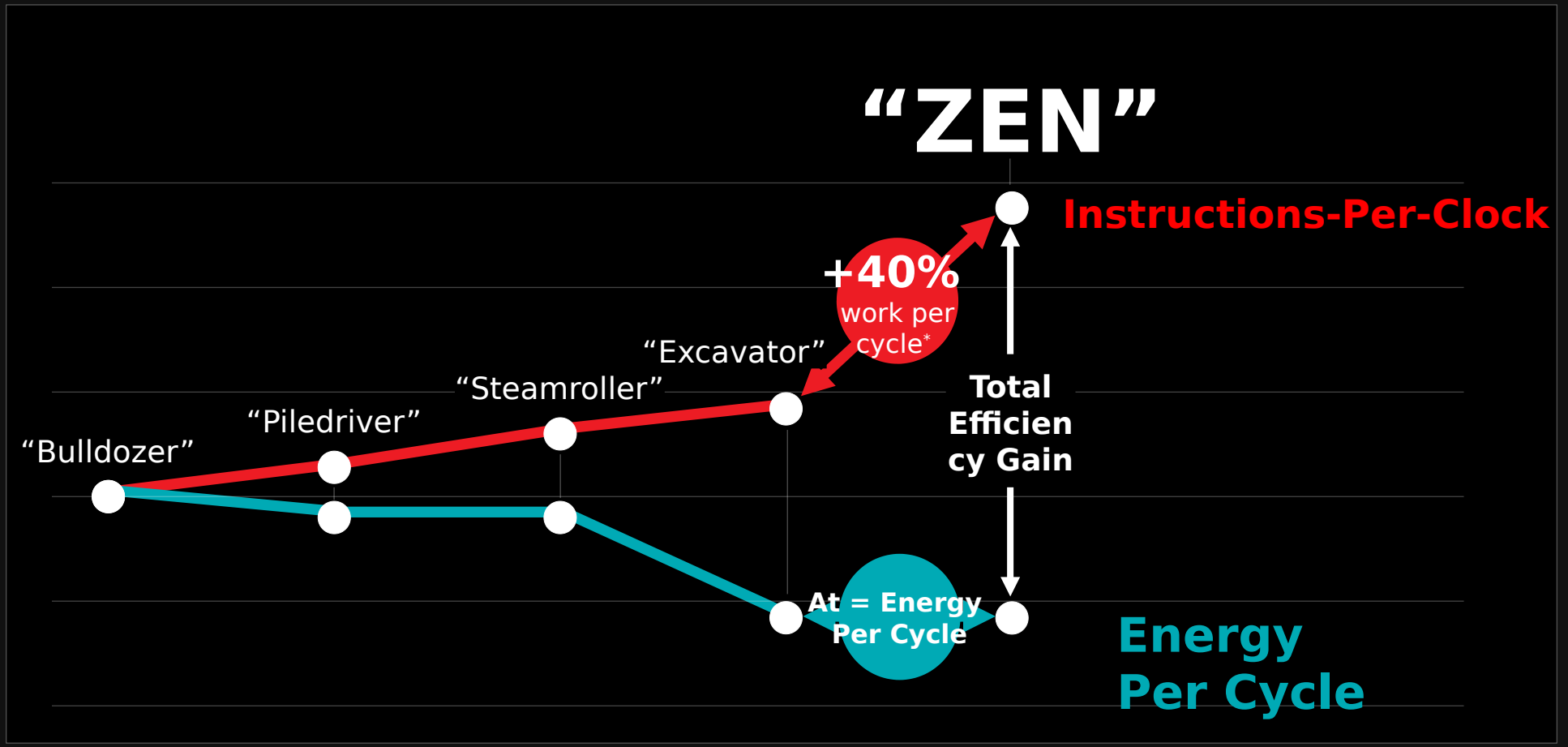
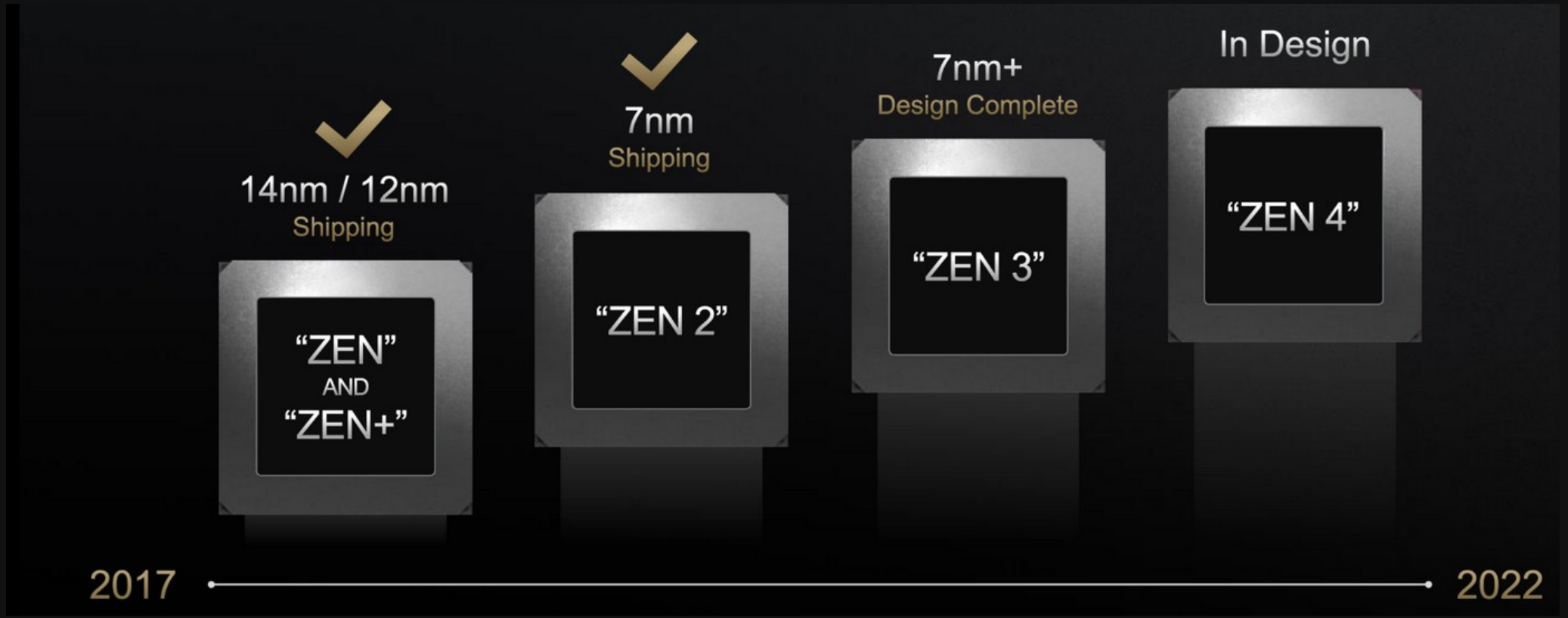
Zen Cores

Zen Design Target



Zen Roadmap

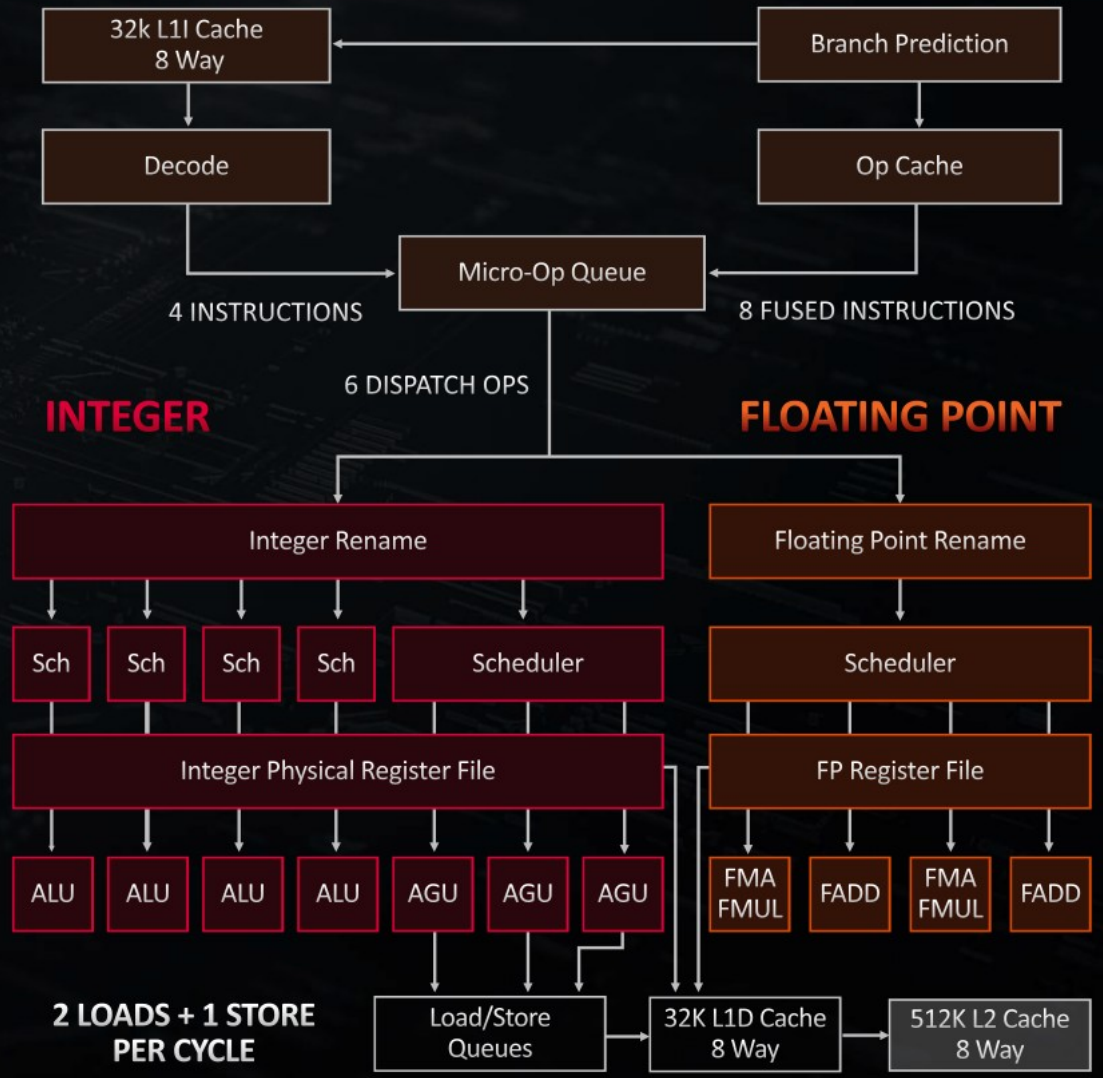

14nm / 12nm
Shipping
“ZEN”
AND
“ZEN+”
7nm
Shipping
“ZEN 2”
7nm+
Design Complete
“ZEN 3”
In Design
“ZEN 4”
2017
2022

"ZEN 2"

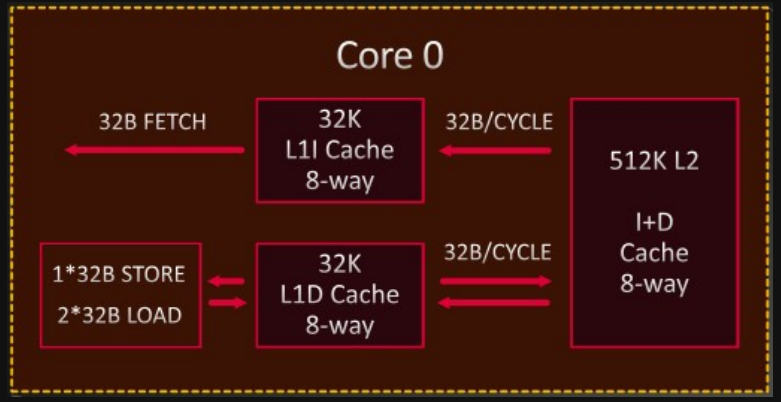
MICROARCHITECTURAL HIGHLIGHTS

- New TAGE branch predictor
- 2x op cache capacity
- Reoptimized L1I cache
- 3rd address generation unit
- 2x FP data path width
- 3x L1 load+store bandwidth
- 2x L3 capacity
- Improved prefetch throttling
- 2 threads per core (SMT) carried forward

15% IPC IMPROVEMENT FROM "ZEN" TO "ZEN 2"



CPU Complex and Cache Hierarchy



- Each core has individual L1-I, L1-D and L2 caches
- There can be up to 4 cores and 16MB of shared L3 cache in a core complex (CCX) - 2 CCX'es are combined into a single CPU chiplet (CCD)

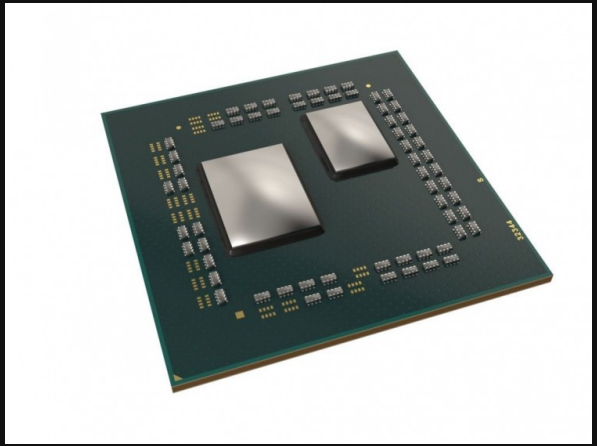
Chiplet Design

Each IP in its Optimal Technology

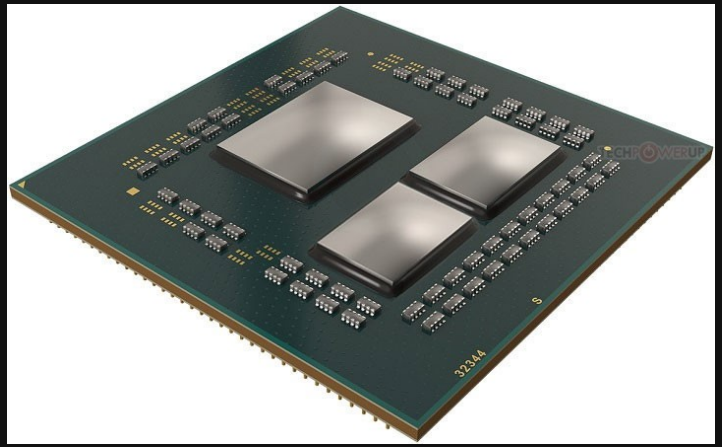
Infinity Fabric™ Enables Modularity (MCM), Scaling (CCD Count)

Optimized I/O Die Enables Common Latency to All Cores/Caches

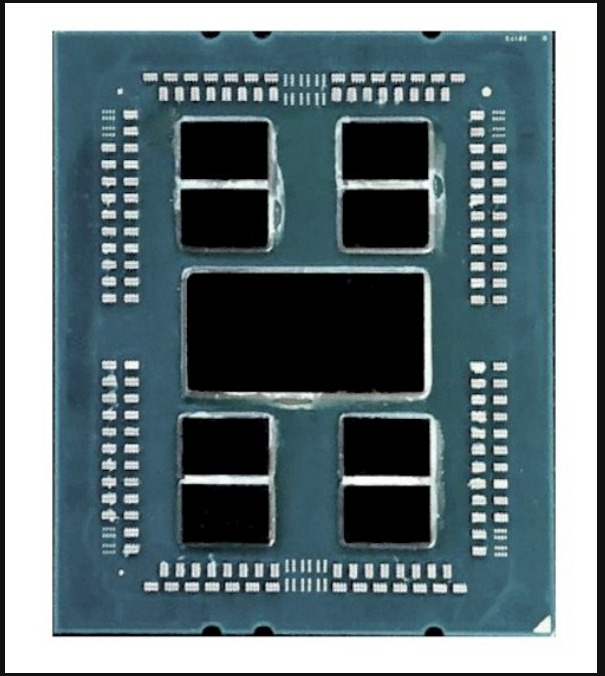
Chiplet Flexibility



Matisse
Single CCD

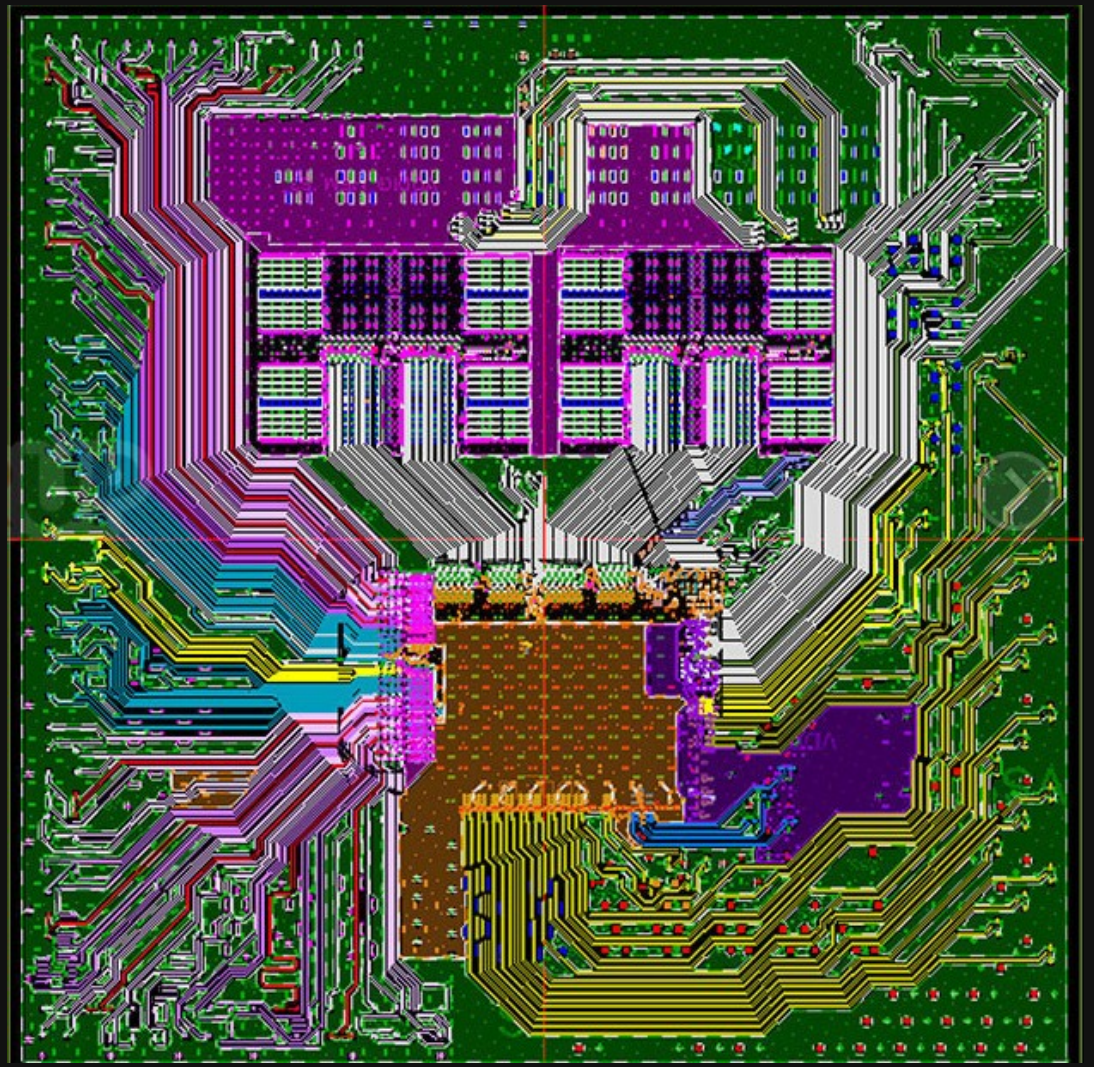


Matisse
Dual CCDs



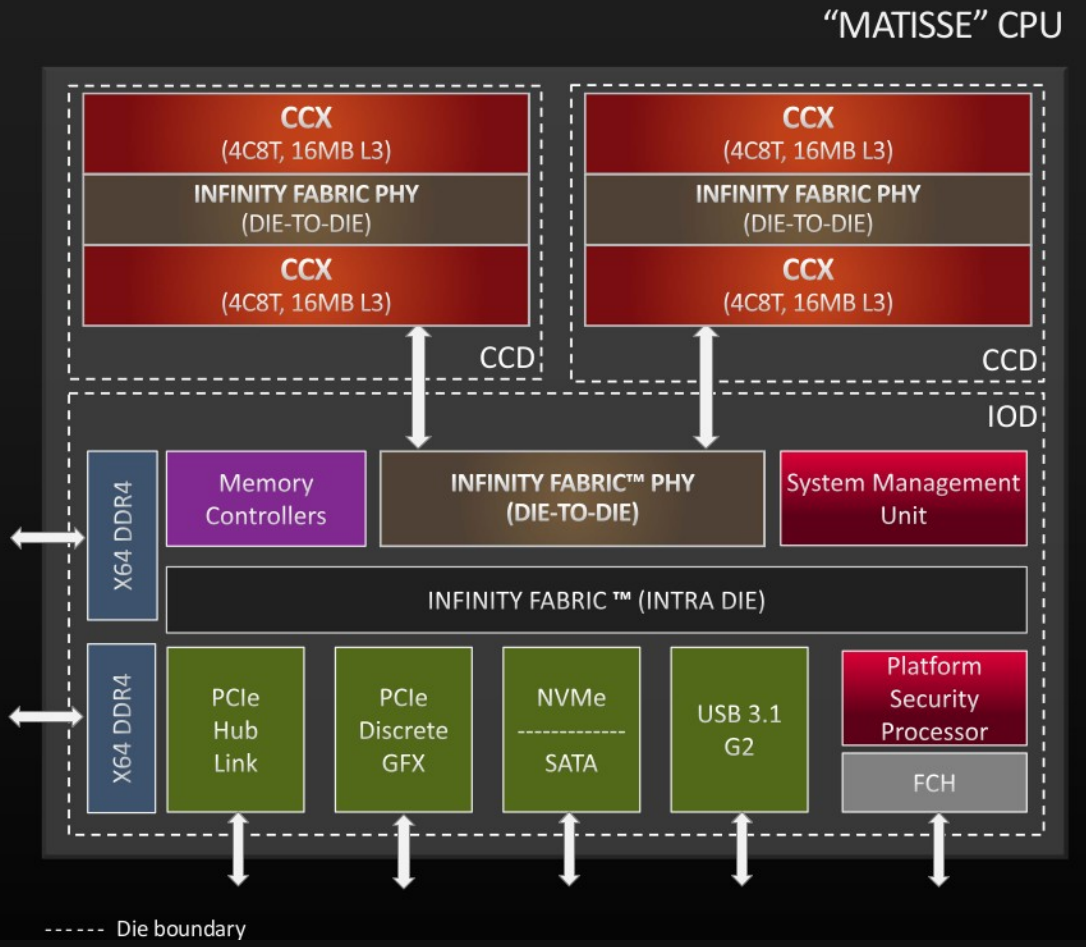
Rome
8 CCDs
Larger IOD

Matisse CPU

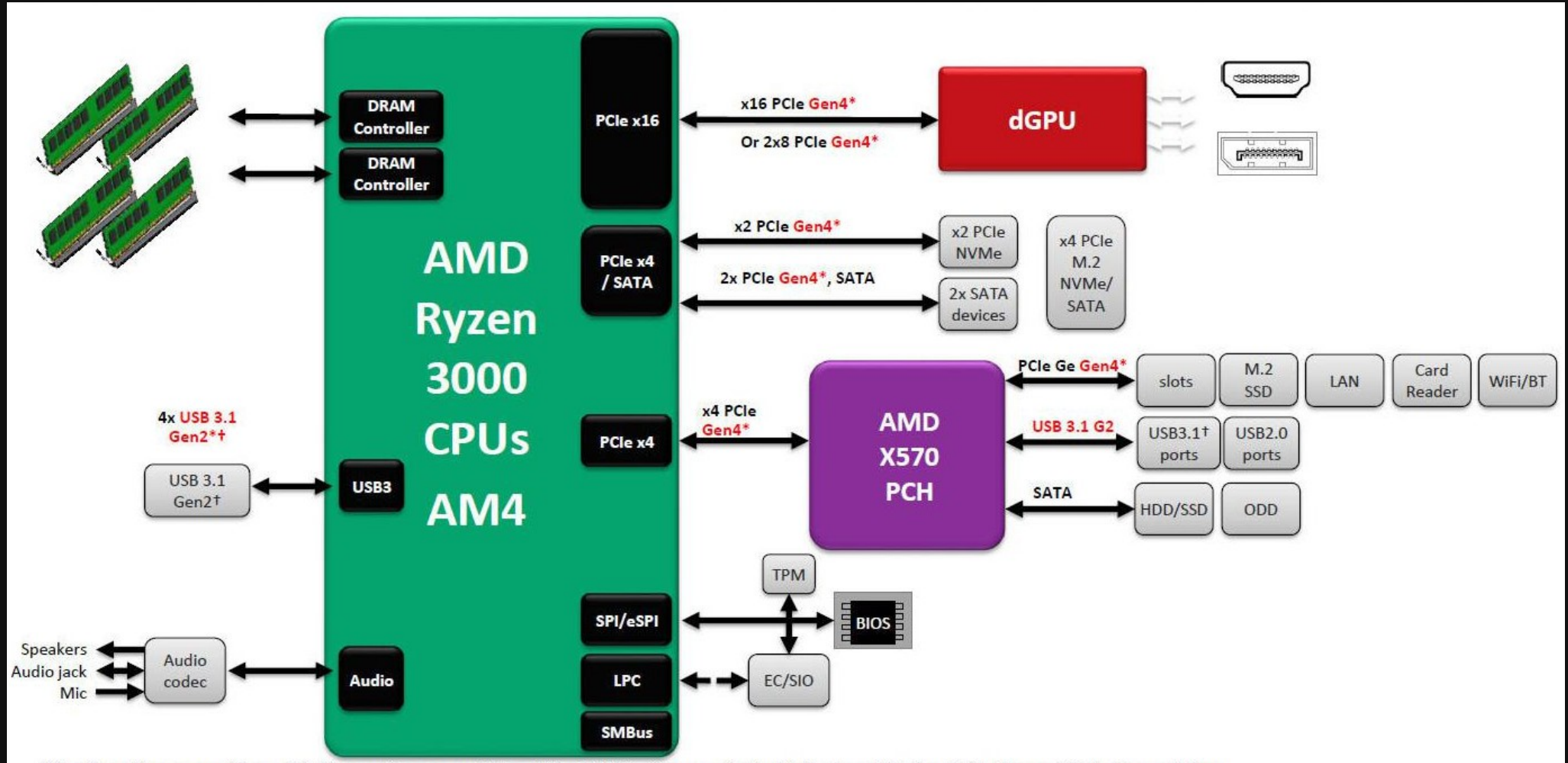


Ryzen 3xxx CPU (“Matisse”)

- A Desktop SoC and a Chipset
  - IOD combined with CCD(s) form the CPU
  - Standalone IOD re-purposed as Chipset
- Leading I/O
  - 48GB/s native PCIe™ BW
  - 4 USB 3.1 10Gb/s ports
- Memory BW
  - 51.2 GB/s Memory BW
  - Dual Channel DDR4 3200 MT/s
- Overclocking
  - Improved Memory overclocking (Phy, Package)
  - De-coupled various IO-die clocks for flexibility
- AM4 Platform Longevity
  - Compatible with AM4 platform



Matisse: System Connectivity



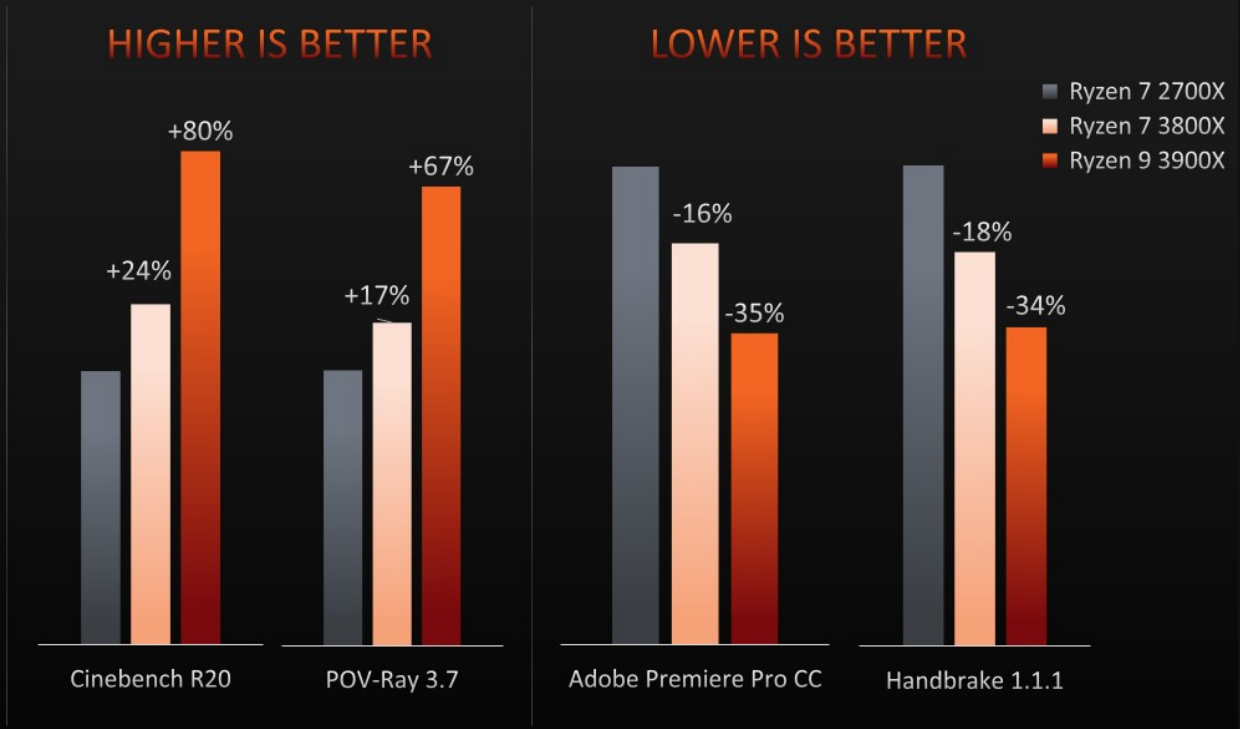
*Configurations vary with model. Diagram is representative of Zen 2 CPUs. Always refer to Motherboard Design Guide for specific implementations.

† Does not support multi-lane or "lane bonding"

Desktop Performance Improvement

Application Performance In Power Efficient TDP

- Compute heavy workloads benefit from power efficient design
- Content Creation, Rendering benchmarks see large gains
- Additional cores in 3900X deliver substantial compute power



Benefits from PCIe Gen4

IO Performance

- Up to 2x PCIe BW vs prior Ryzen generation

Storage Performance

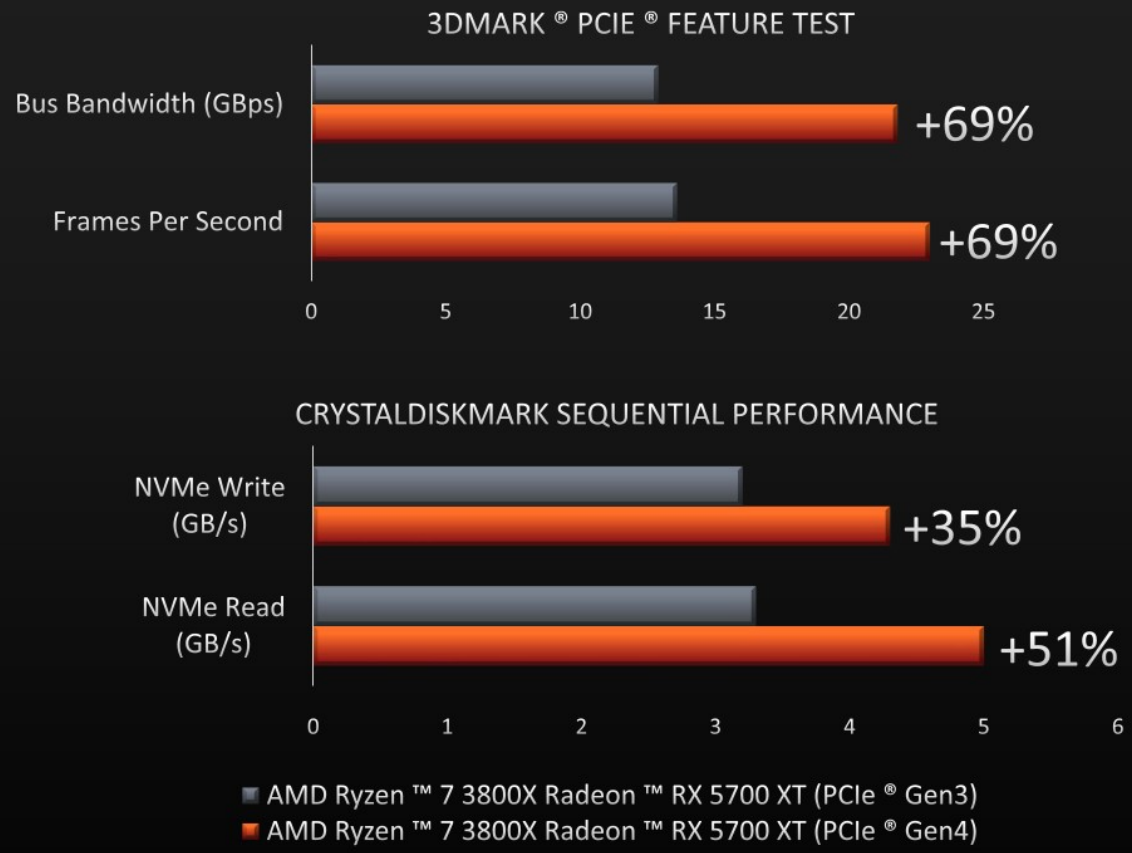
- Large Block Sequential accesses are severely limited by link speeds

3DMark® PCIe Feature Test

- Vertex animation (game VFX) is sensitive to bus bandwidth, allowing significant upside

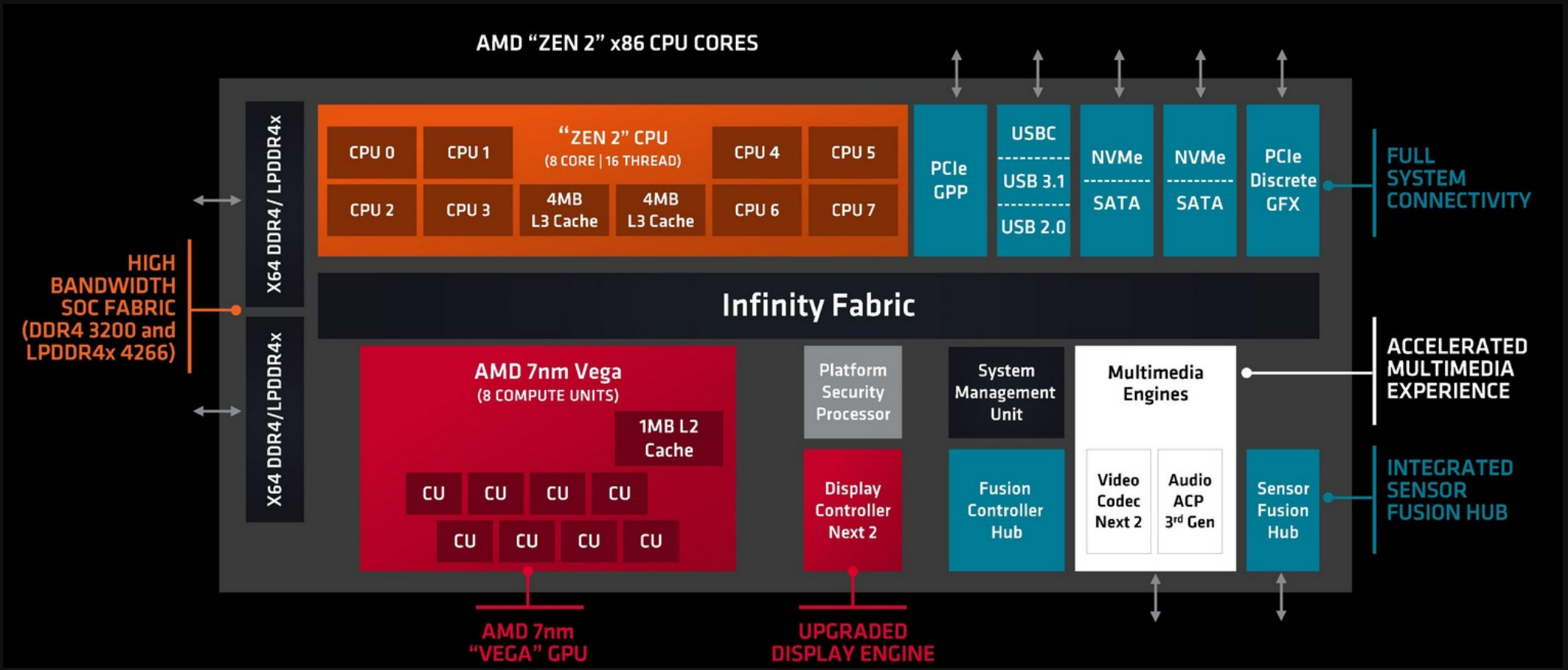
DaVinci Resolve

- Bus bandwidth is a significant limiting factor for non-linear editing (NLE) performance

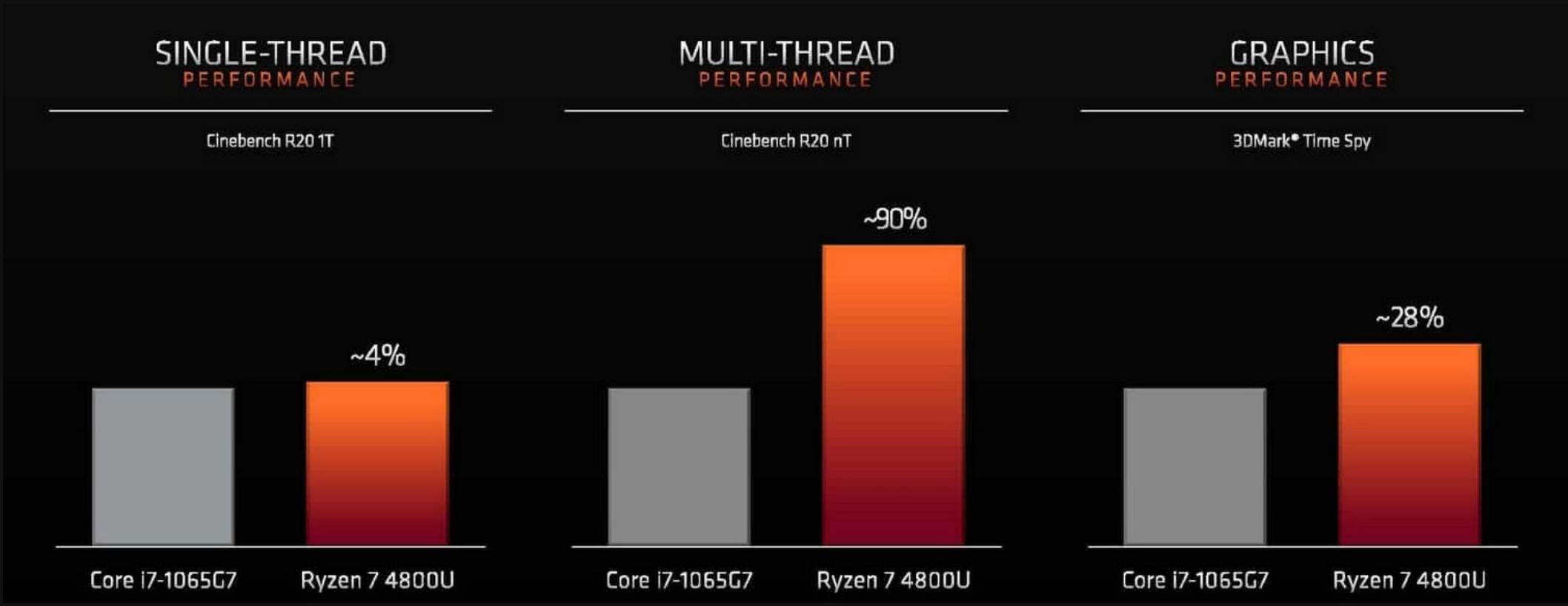


Renoir APU

Ryzen 4xxx APU (“Renoir”)



CPU performance



Laptop iGPU Gaming Performance

More questions?

Backup

Old “Integrated Graphics” Architecture