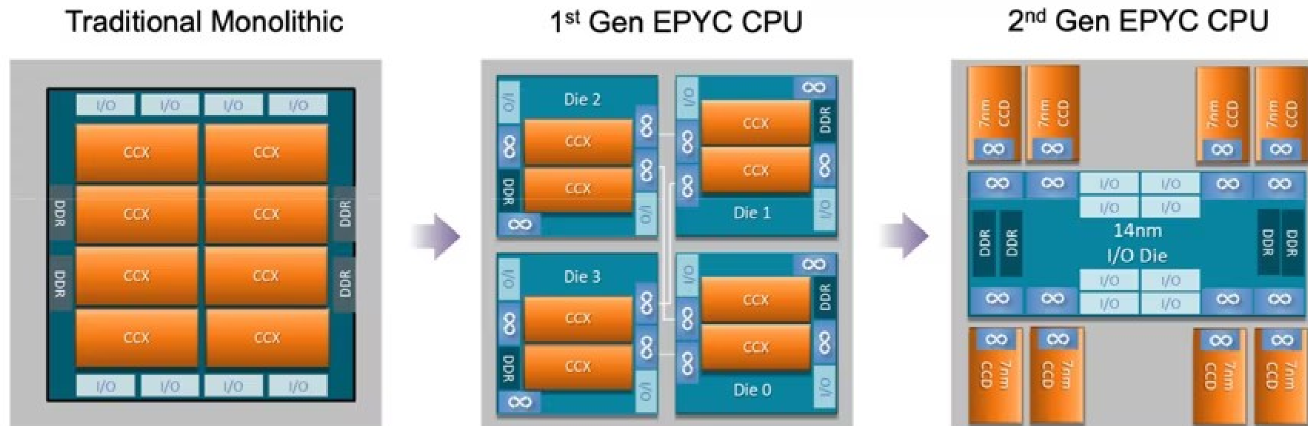
UCIe Chiplet Standard

BLU October, 2023

Shankar Viswanathan

What is a chiplet?

- A chiplet is a silicon die with a defined set of features along with an interface to connect to other chiplets
- Multiple chiplets are combined into a single package to provide the full functionality of the product



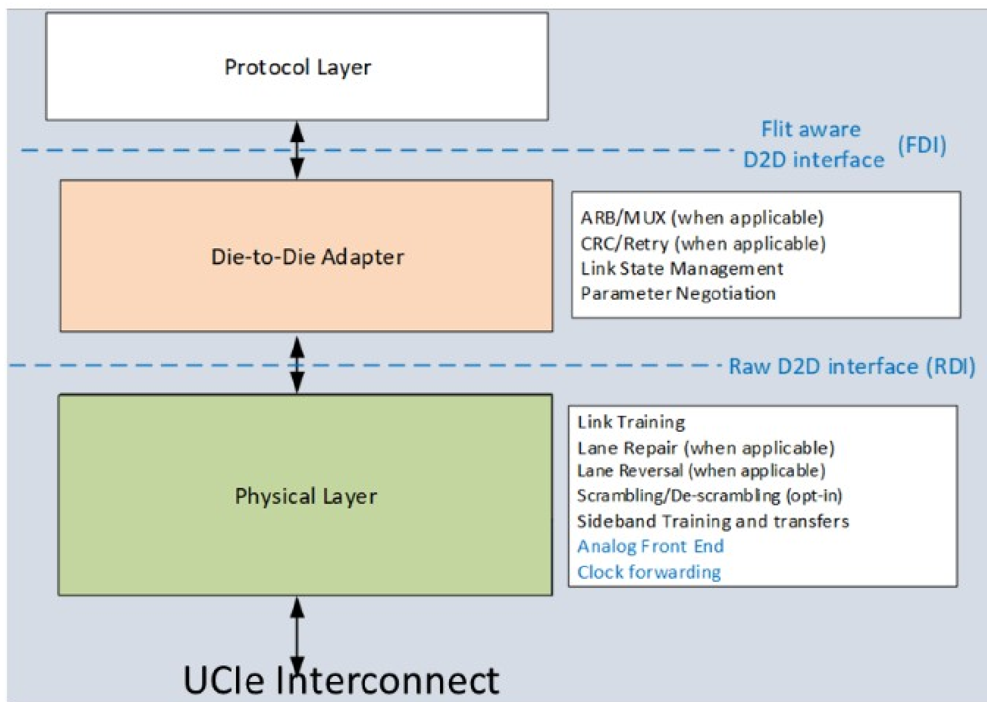
Why chiplets?

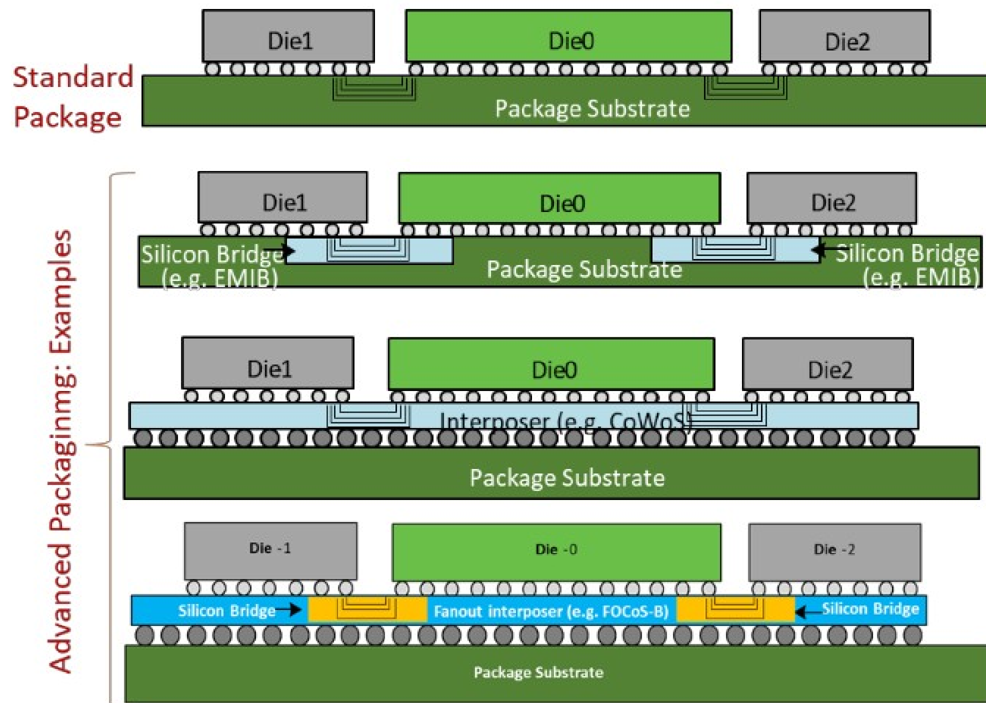
- Lower cost: Chiplets are generally smaller and have better yield compared to large monolithic chips. Known good die used for packaging
- Reusable: Chiplets could be reused across multiple products
- Composable: Chiplets can be combined in different ways to create various SKUs
- Process optimization: chiplet could be fabricated on a process that is most optimal for that logic (power, performance, area/cost)

UCIe

- Universal Chiplet Interconnect Express
- Open specification for die-to-die connections between chiplets – primary goal is to enable use of chiplets from different vendors in a single package
  - https://www.uciexpress.org
- Initially developed by AMD, ARM, GCP, Intel, Meta, Qualcomm, Samsung, TSMC, etc. (NVIDIA joined later)
- Version 1.0 released in early 2022, 1.1 in August 2023

UCIe Transport and Packaging



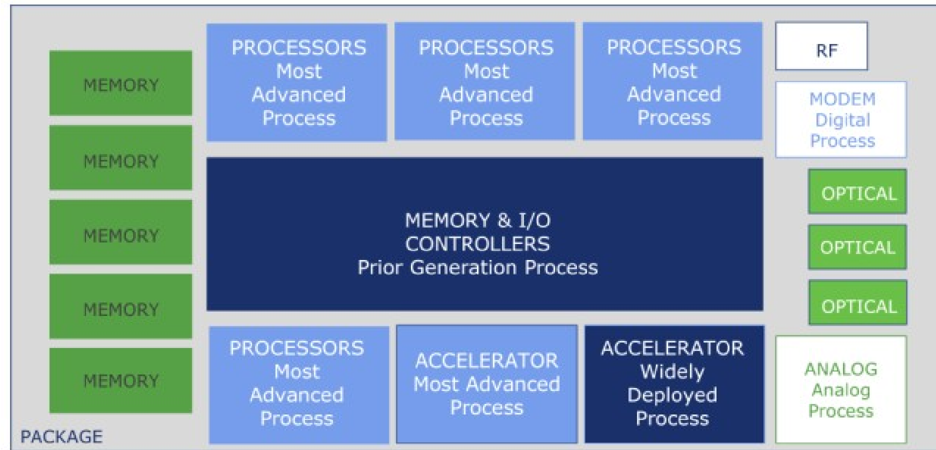


Source: UCIe whitepaper

Protocols

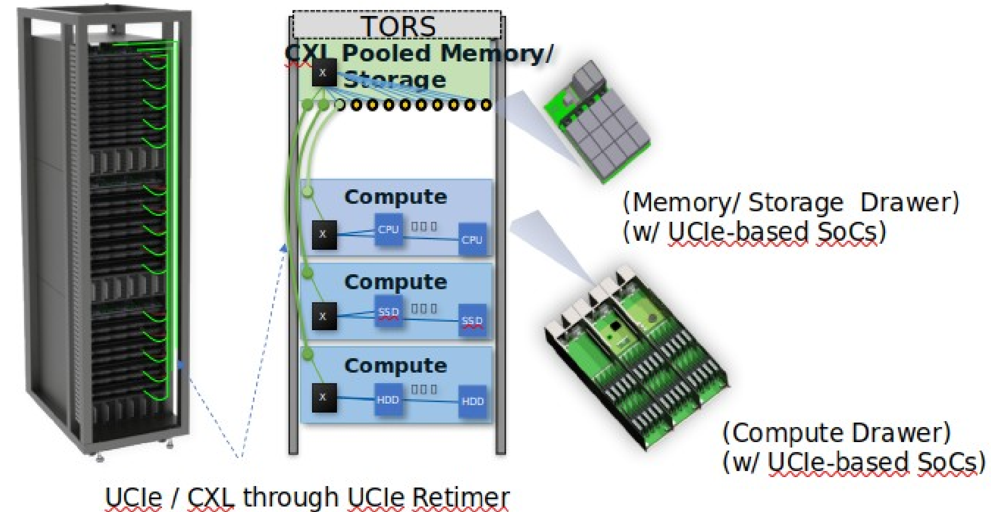
- UCIe natively maps PCIe and CXL (io, mem, and cache)
- Also defines streaming protocol to map other protocols
- Work continues to define other protocols based on current and future use cases

UCIe Usage Models



SoC Package level construction for wide range of usages from Hand-held to high-end servers

✓ Mix and match dies from multiple sources with different packaging options



Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics, electrical cable, mmWave)

Source: UCIe whitepaper

UCIe characteristics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 - 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 - 224	165 - 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G - 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

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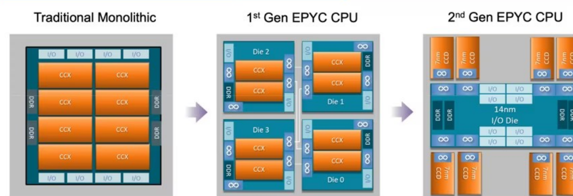

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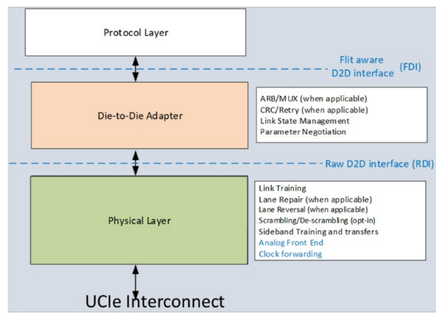

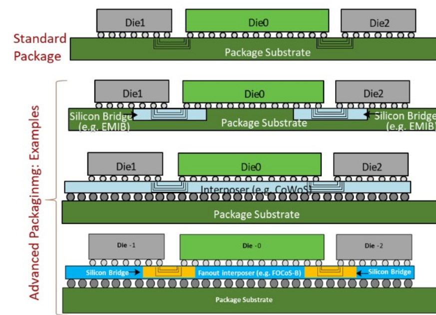

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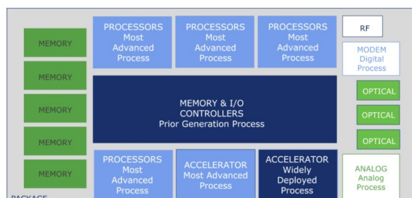

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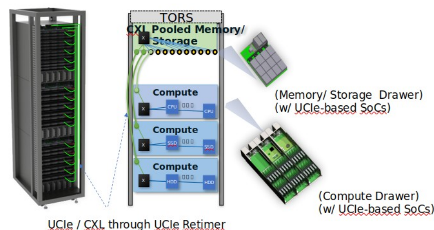

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